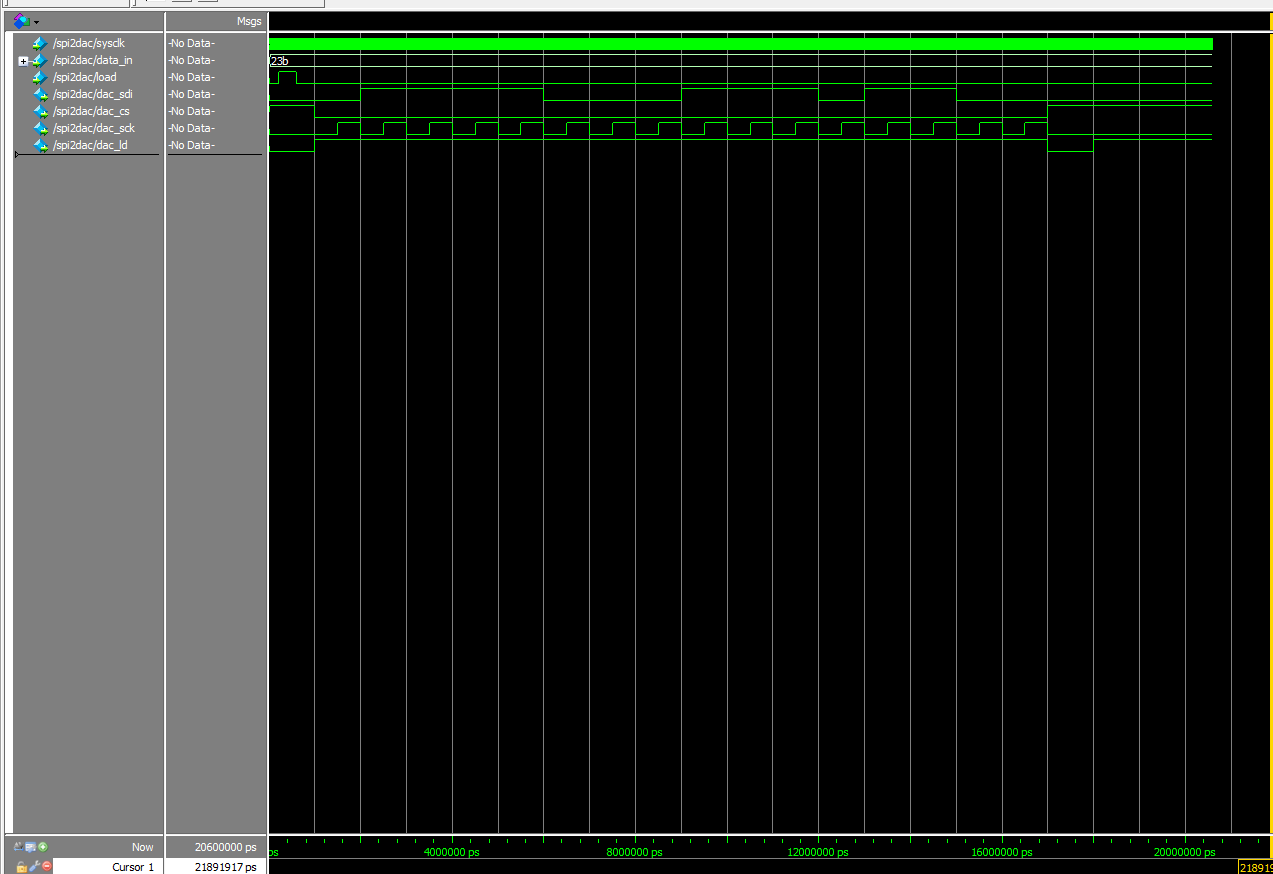
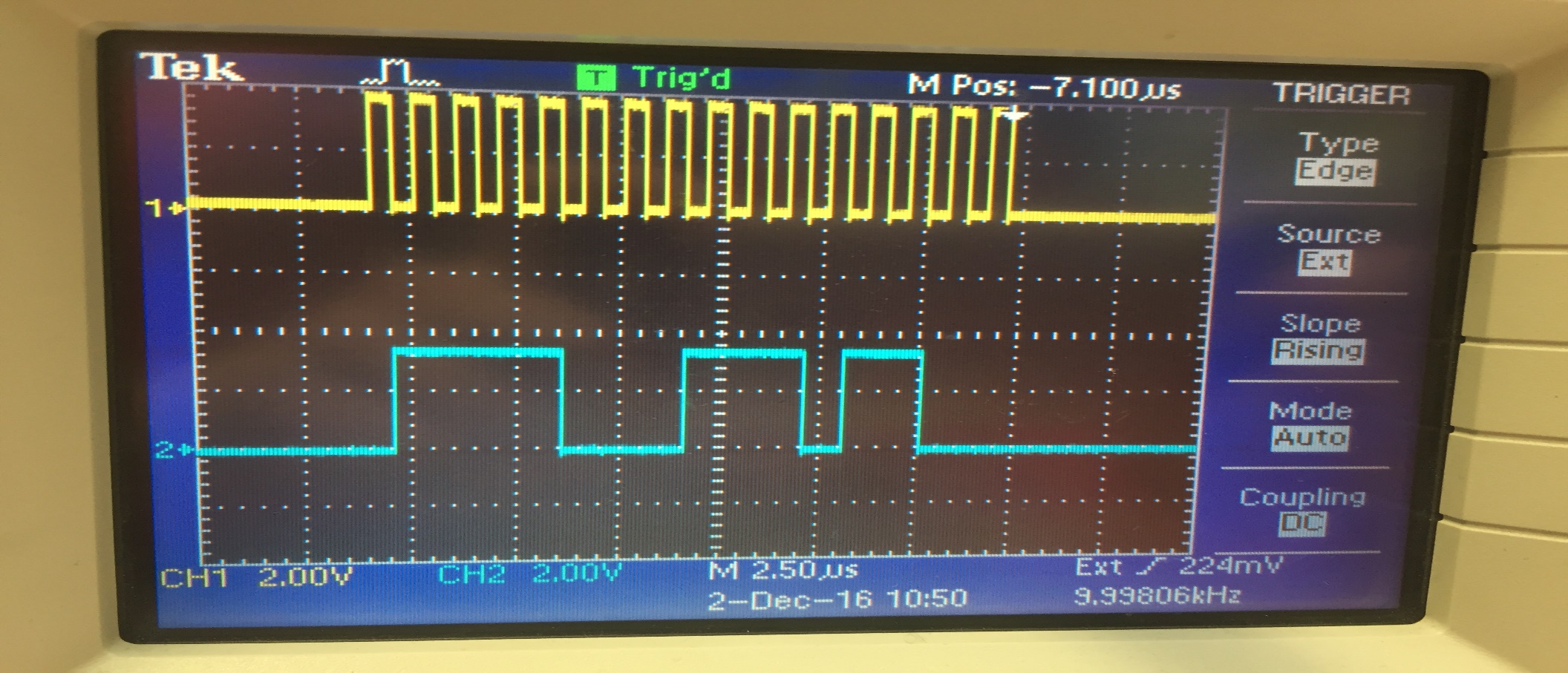
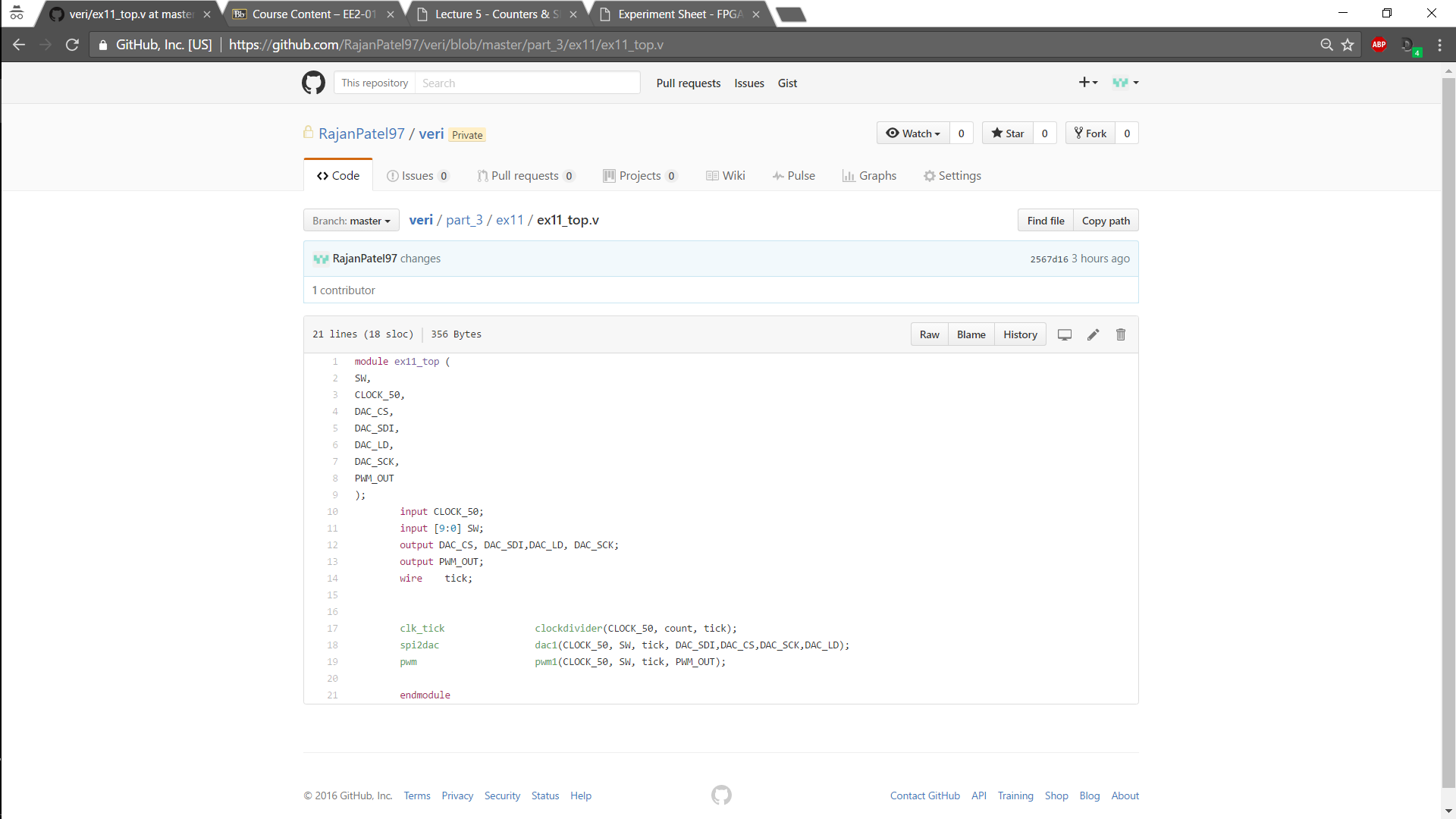
Verilog Experiment - Part 3

Experiment 10

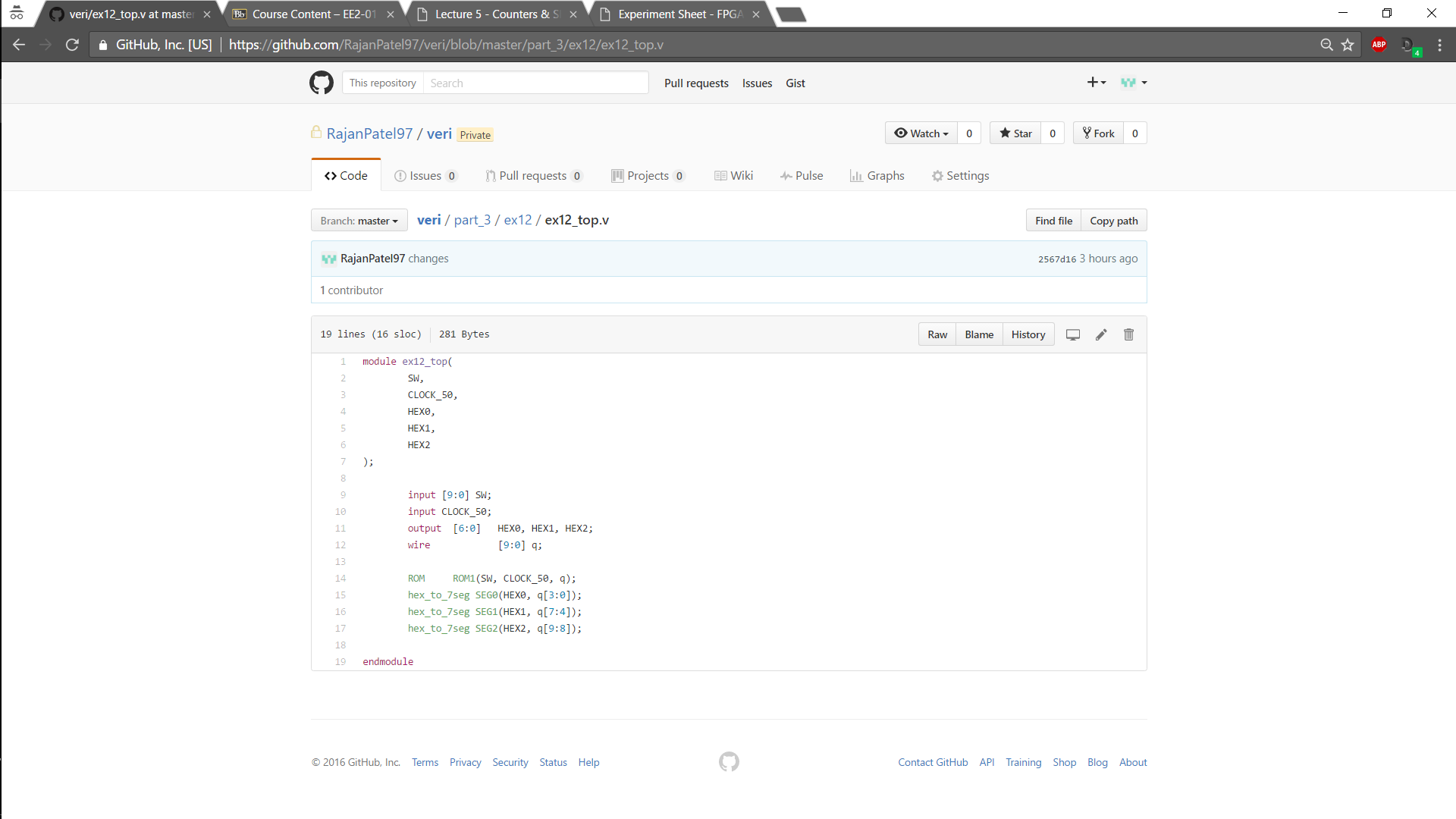


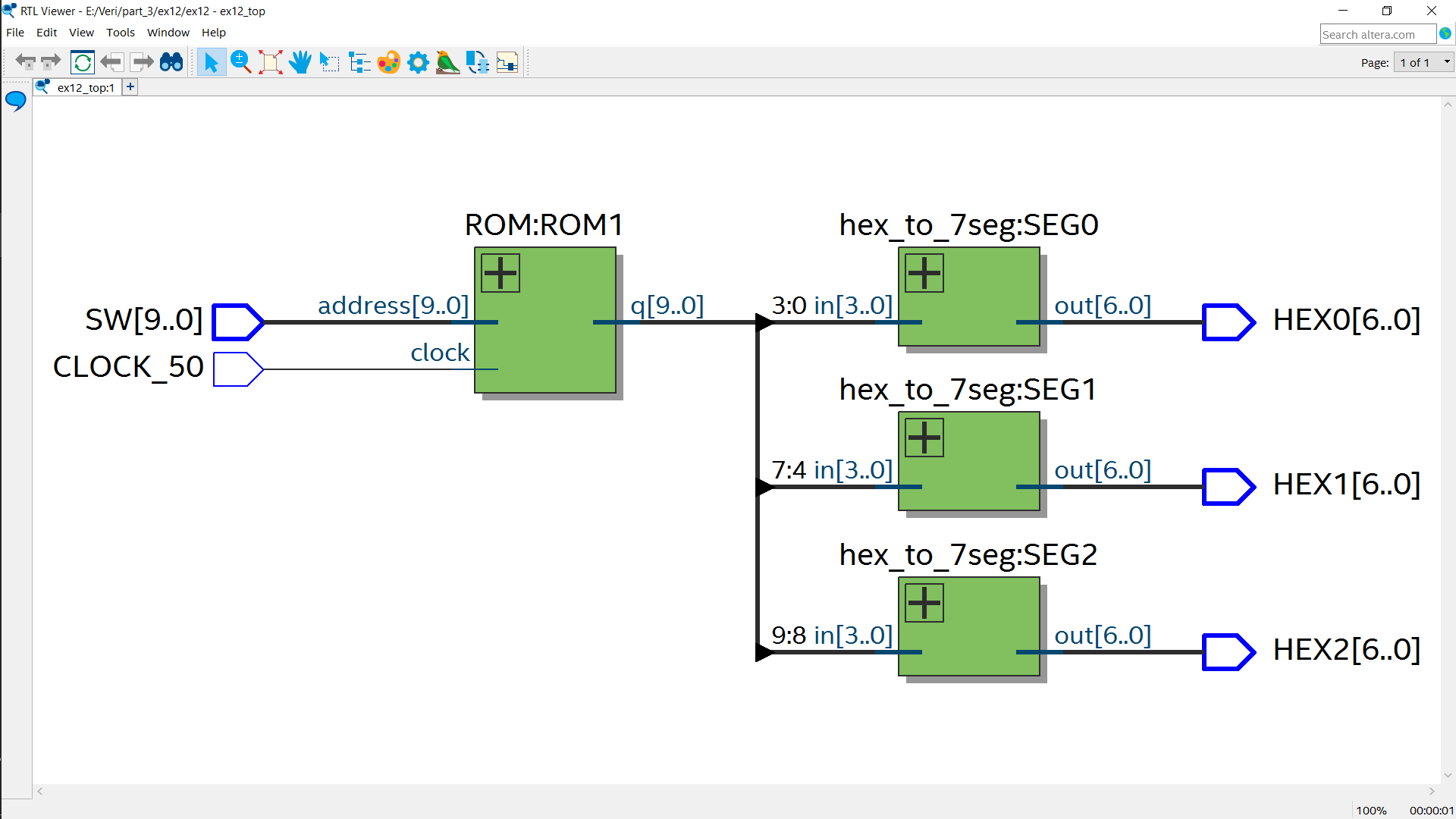
Voltage range was fine

Experiment 11

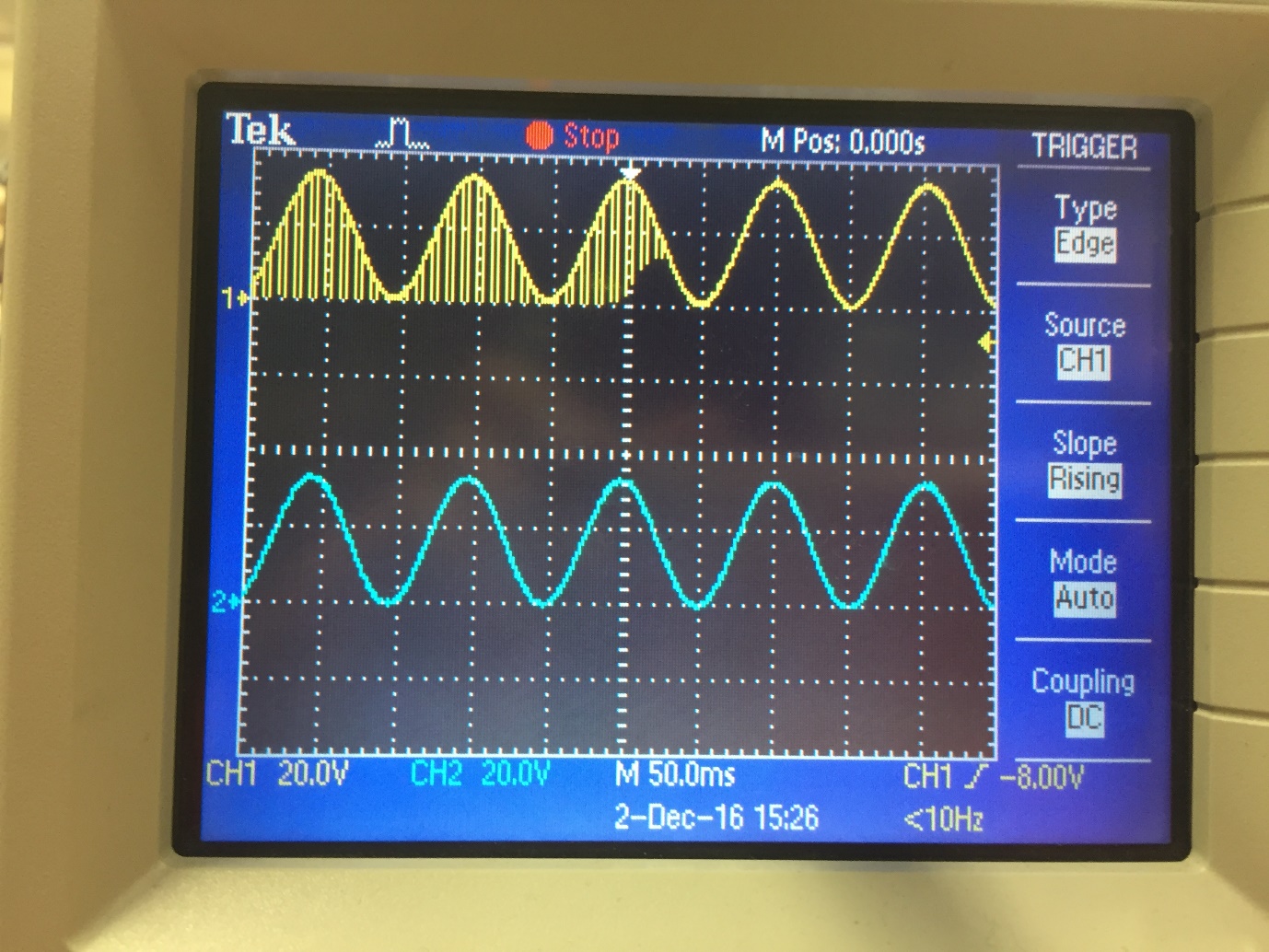


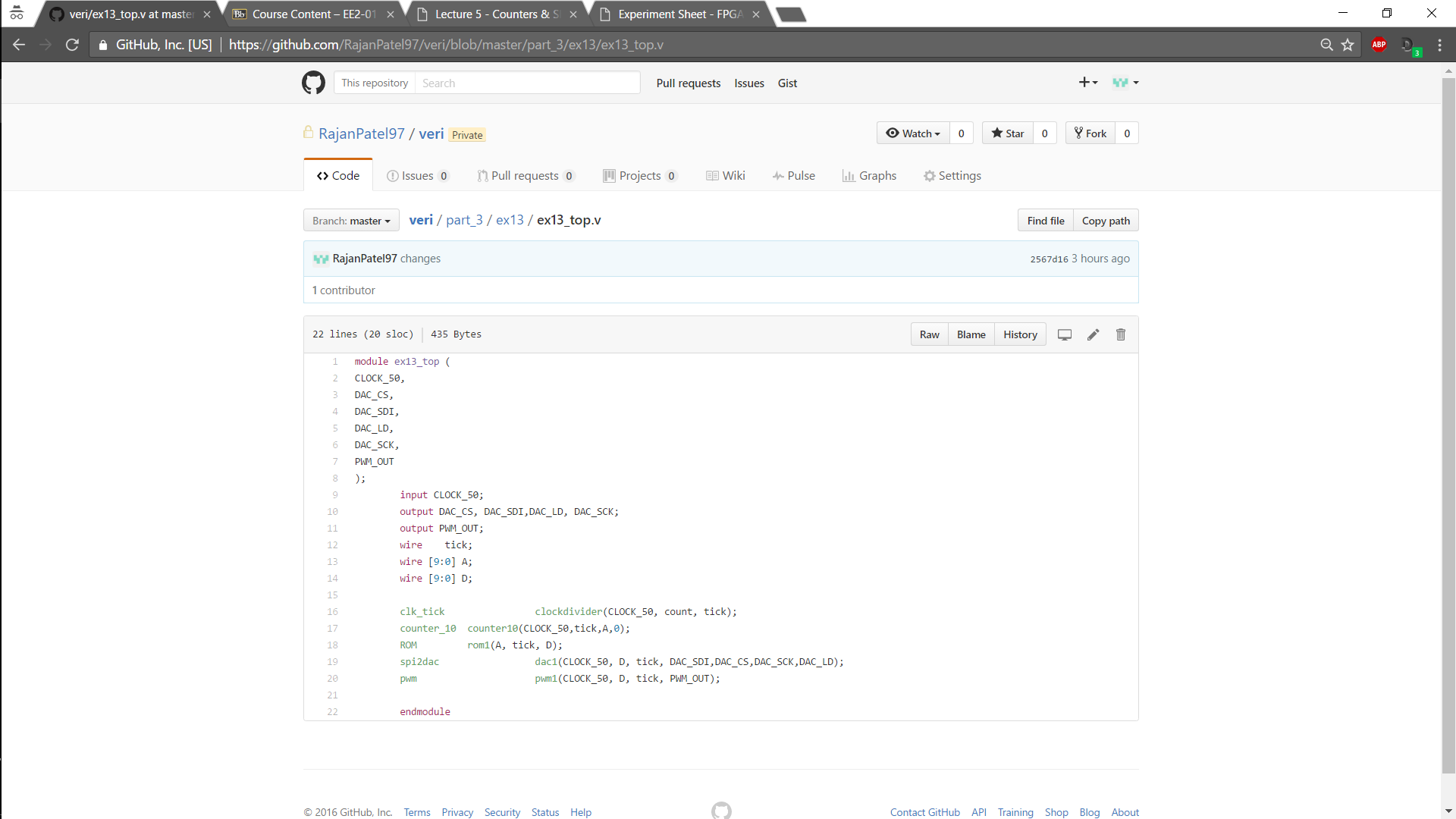
Experiment 12

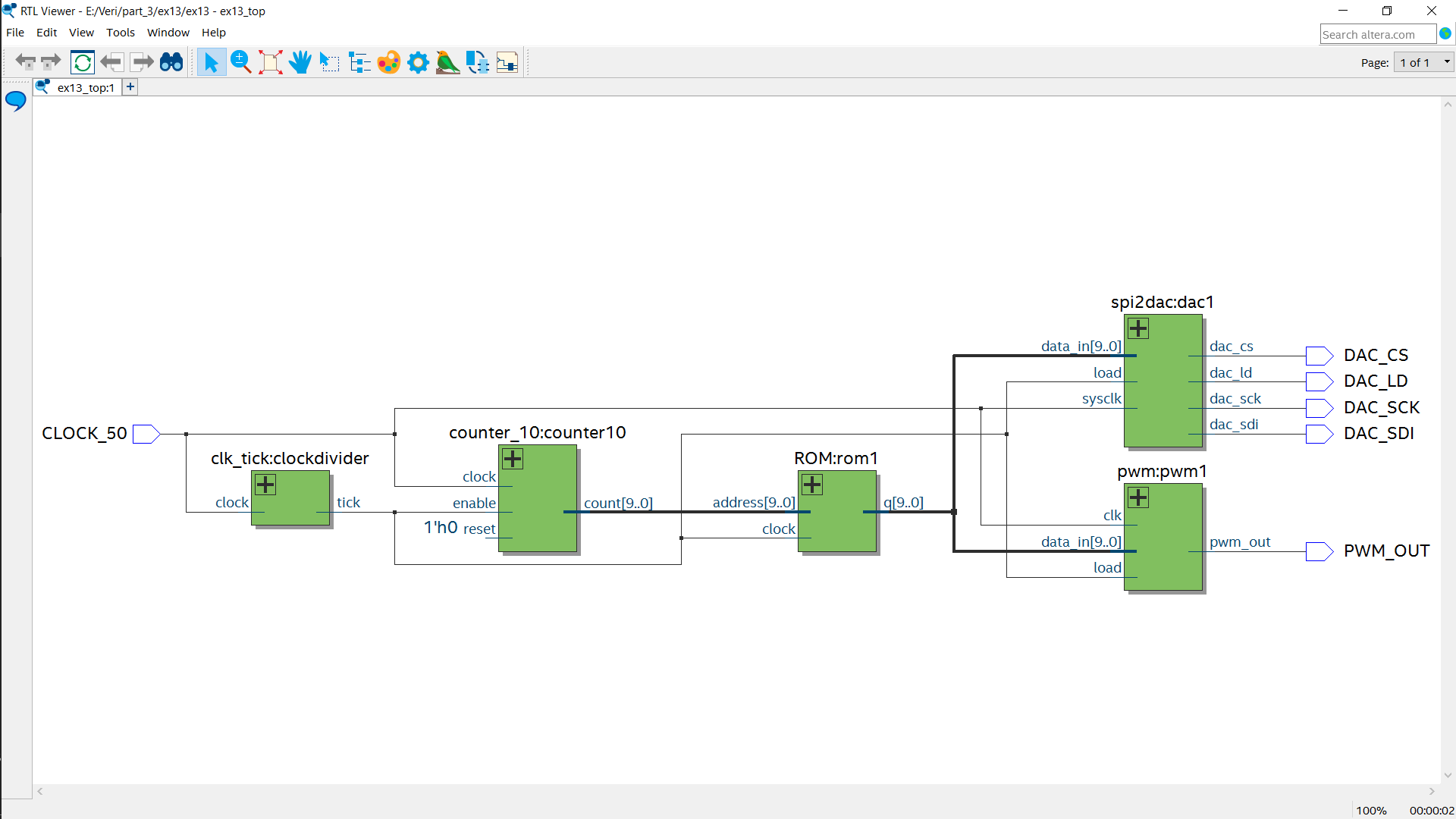




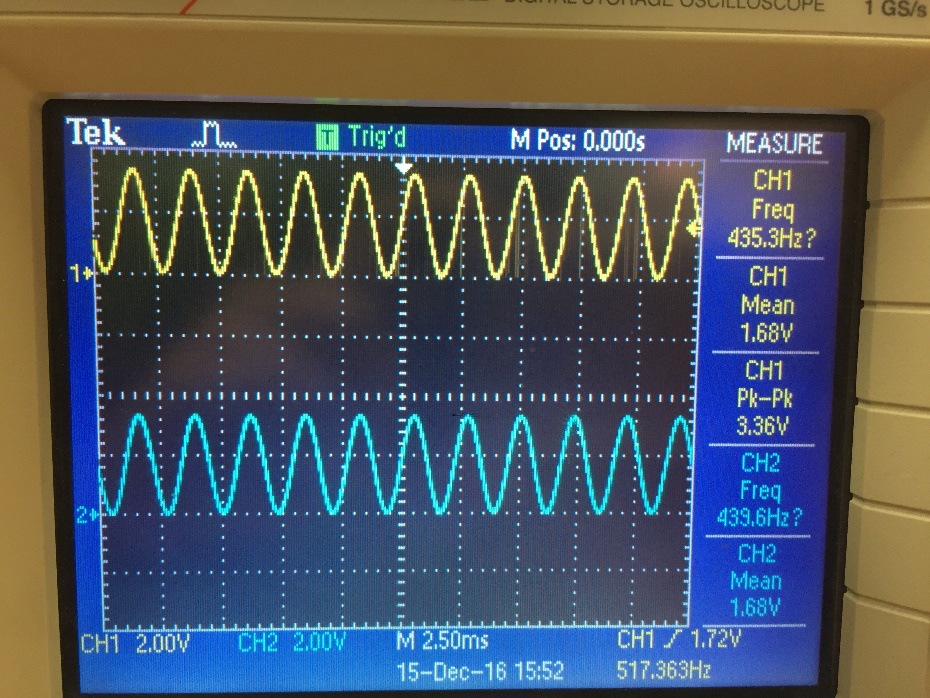
Experiment 13

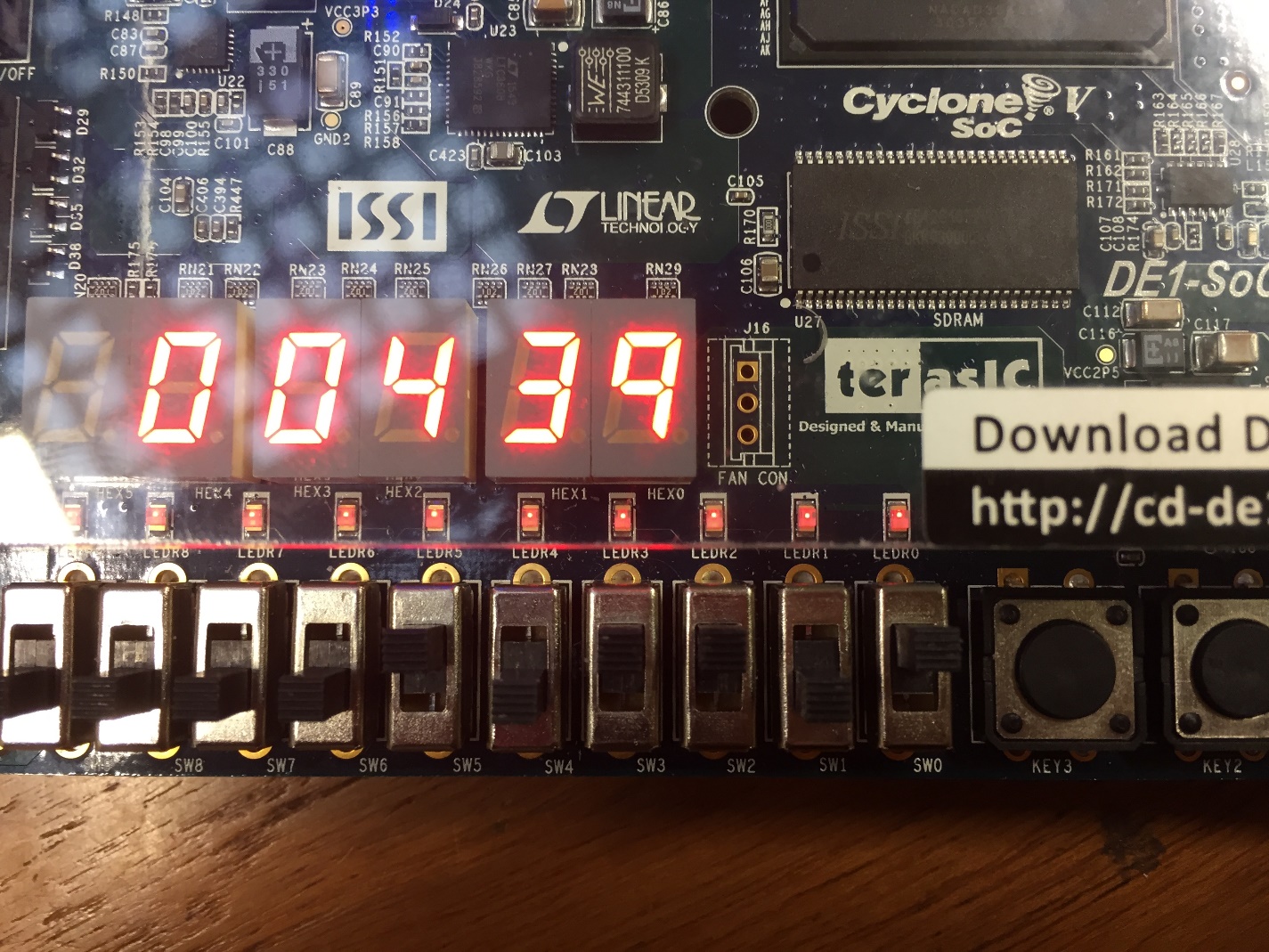


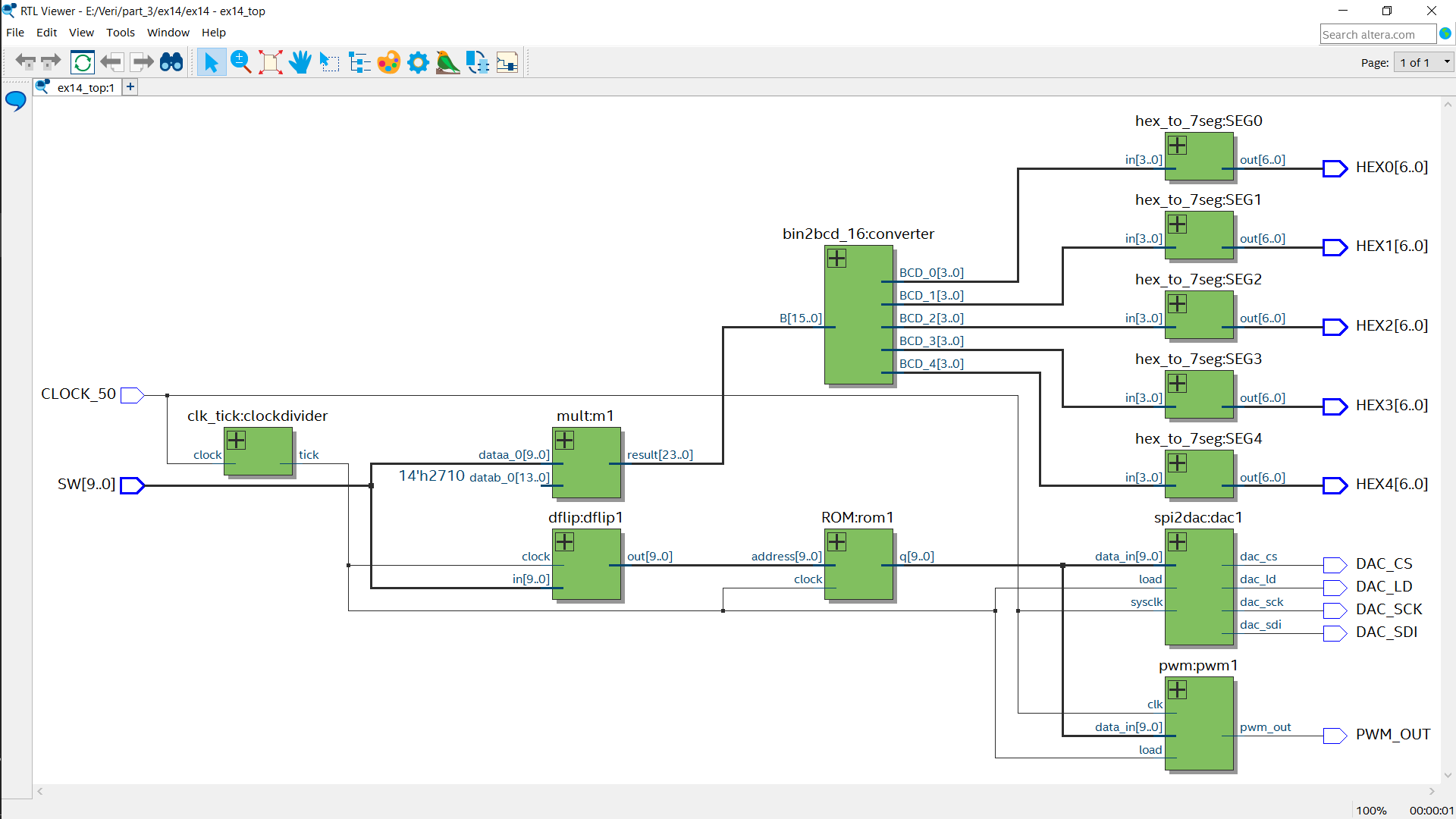


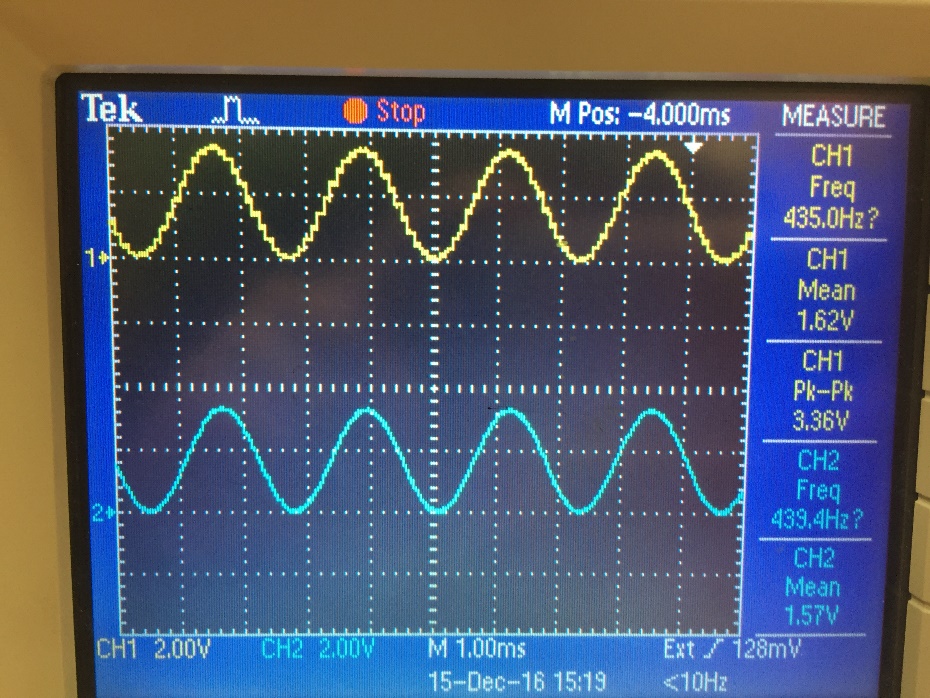


Experiment 14 & 15 (Optional Challenge)







Experiment 15 (Optional)

